# DATA SHEET

# PCD5095
# DECT baseband controller

Objective specification
File under Integrated Circuits, IC17

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Philips
Semiconductors

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**CONTENTS**

## 1 FEATURES

- 80C51 ports P0, P1, P2 and P3 available for interfacing to display, keyboard, $I^2C$-bus, interrupt sources and/or external memory. Integrated 64 kbyte ROM, 3 kbytes of data memory and 1kbyte System Data RAM. External program memory is addressable up to 128 kbytes
- +2.7 to 5 V port (P0 to P3) interface
- TDMA frame (de)multiplexing, transmission or reception can be programmed for any slot
- Ciphering, scrambling, CRC checking/generation and protected B-fields
- Speech and data buffering space for six handsets
- Local call and B-field loop-back
- Two interrupt lines for BML and DSP to interrupt 80C51
- On-chip, three channel time-multiplexed 8-bit Analog-to-Digital Converter (ADC) for RSSI measurement, one for battery voltage measurement and one channel available for other purposes
- On-chip 8-bit Digital-to-Analog Converter (DAC) for electronic potentiometer function
- Phase error measurement and phase error correction by hardware
- DACs and ADCs for dynamic earpiece and dynamic or electret microphone
- On-chip reference voltage
- On-chip supply for electret microphone
- Very low ohmic buzzer output
- Serial interface to external ADPCM CODEC (PCD5032) or 8 kHz u-law samples
- Speech switch for Digital Telephone Answering Machine (DTAM) connected to SPI interface
- IOM®-2 interface (Siemens registered trademark)
- Serial interface to synthesizer for frequency programming
- Programmable polarity and timing of radio-control signals
- GMSK pulse shaper
- On-chip comparator for use as data-slicer
- Easy interfacing with radio circuits, operating at other supply voltage (RF supply pin with level shifter for RF signals)
- Low-power oscillator with integrated frequency adjustment
- QFP100 package
- Power-on-reset
- Programmable power-down modes
- Low supply voltage (2.7 to 3.6 V)
- CMOS technology.

### 1.1 DSP software features

- 3x ADPCM transcoding complying with G.726
- A-Law encoding and decoding complying with G.711
- 4 Channel bidirectional ADPCM interface to the IOM®-2 and radio interface
- Programmable channel switching and buffers
- Channel mute.

For each DSP software version a separate manual is available in which detailed information is provided on how parameters must be set. For further information please contact Philips Semiconductors.

## 2 GENERAL DESCRIPTION

The PCD5095 is designed for GAP-compliant business systems, PABX and WLL. Two modes can be selected: three channel ADPCM CODEC with conversion of ADPCM samples to linear PCM format and vice versa, the second mode copies four ADPCM samples into two IOM data buffers and vice versa. In both modes the DSP controls the bidirectional data flow from the radio interface and the IOM®-2 interface. The 80C51 controls the DECT protocol and the IOM®-2 interface. The performance of the embedded 80C51 microcontroller is twice the performance of the classic architecture. The PCD5095 has 64 kbytes of PROM program memory and 3 kbytes of data memory on-chip. In addition there is 1 kbyte of on-chip data memory that is shared with the Burst Mode Logic (BML), the DSP and the System Data RAM (SDR).

## 3 ORDERING INFORMATION

| TYPE NUMBER | PACKAGE | | |
|---|---|---|---|
| | NAME | DESCRIPTION | VERSION |
| PCD5095H | QFP100 | plastic quad flat package; 100 leads (lead length 1.95 mm); body $14 \times 20 \times 2.8$ mm | SOT317-2 |

## 4 BLOCK DIAGRAM

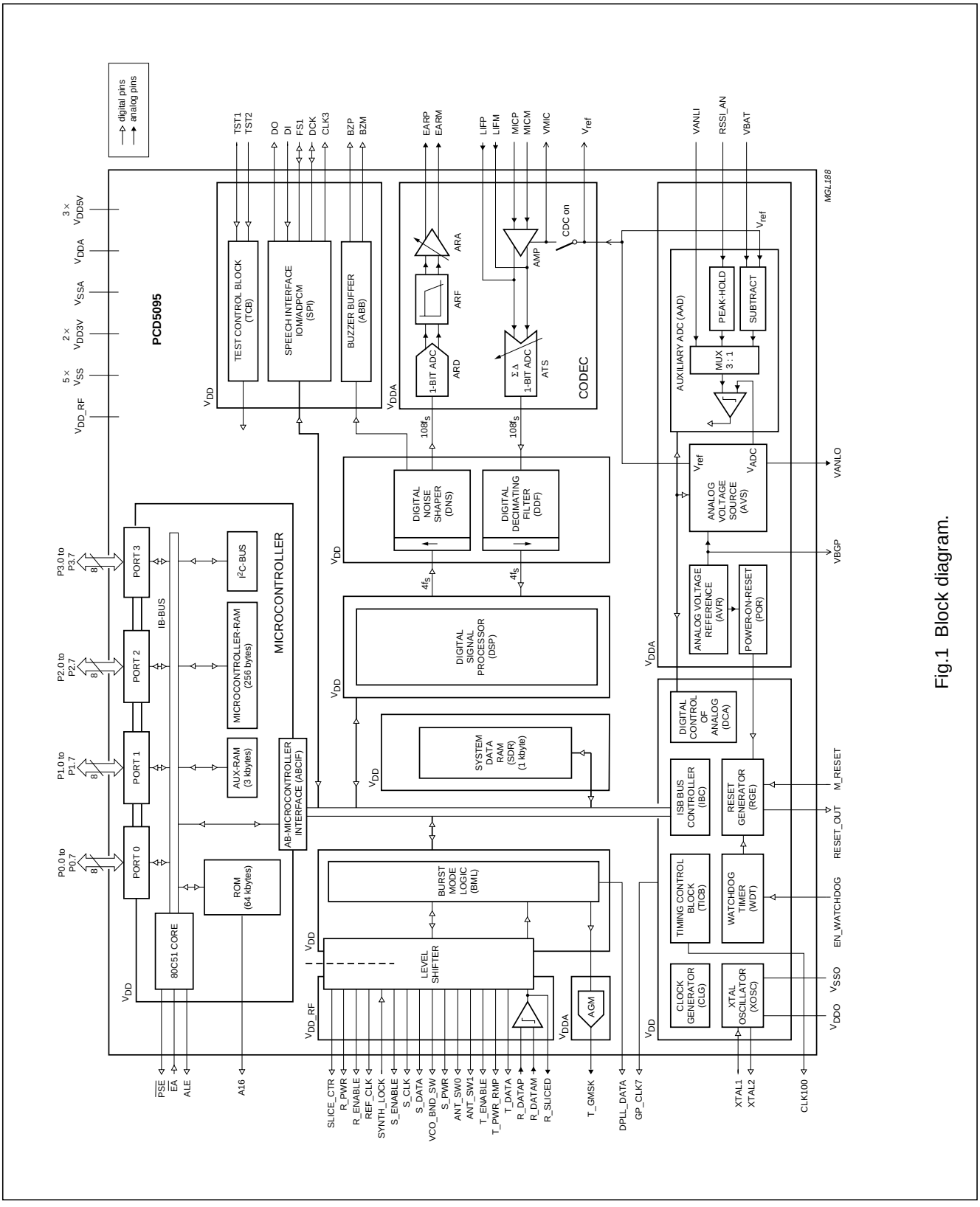



Fig.1 Block diagram.

## 5 PINNING INFORMATION

### 5.1 Pinning

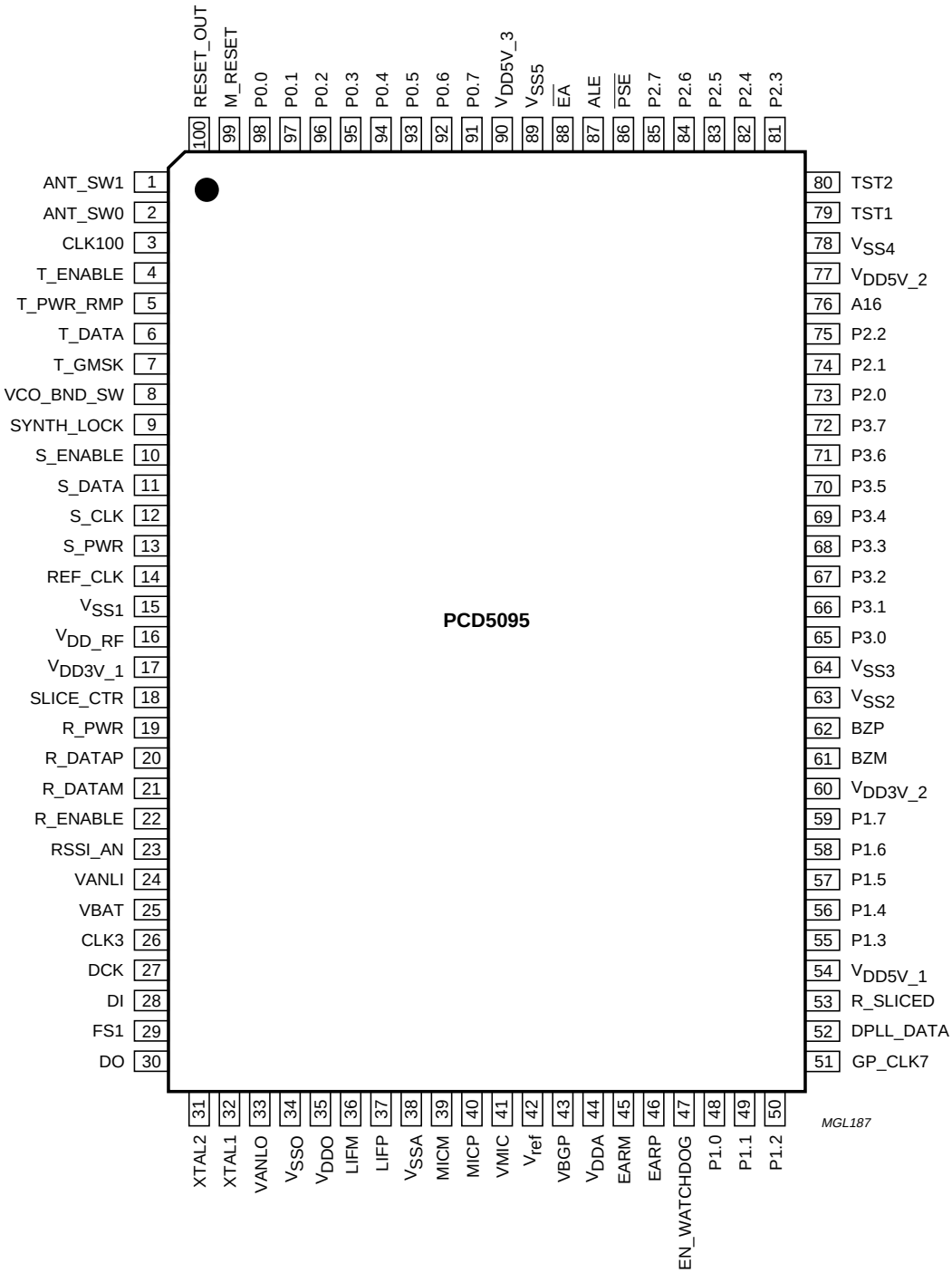



Fig.2 Pin configuration (QFP100).

### 5.2 Pin description

**Table 1** QFP100 package

| SYMBOL | PIN | I/O | STATE AFTER RESET | PIN TYPE | PIN DESCRIPTION |
|---|---|---|---|---|---|
| ANT_SW1 | 1 | O | H | ISP2DRF3 | antenna switch 1 output |
| ANT_SW0 | 2 | O | H | ISP2DRF3 | antenna switch 0 output |
| CLK100 | 3 | O | H | ISP2DPES | 100 Hz signal related to DECT frame timing output |
| T_ENABLE | 4 | O | H | ISP2DRF3 | enable transmitter output |
| T_PWR_RMP | 5 | O | L | ISP2DRF3 | switch transmitter power output |
| T_DATA | 6 | O | off | ISF2DRF3 | unmodulated transmitter data output |
| T_GMSK | 7 | O | L | ANAIOD1 | GMSK modulated transmitter data output |
| VCO_BND_SW | 8 | O | L | ISP2DRF3 | VCO band switch output |
| SYNTH_LOCK | 9 | I | – | DIPP0RF3 | synthesizer lock input |
| S_ENABLE | 10 | O | L | ISP2DRF3 | synthesizer enable output |
| S_DATA | 11 | O | L | ISP2DRF3 | serial synthesizer data output |
| S_CLK | 12 | O | L | ISP2DRF3 | clock for serial synthesizer interface output |
| S_PWR | 13 | O | H | ISP2DRF3 | switch synthesizer power output |
| REF_CLK | 14 | O | running | ISP4DRF3 | 13.824 MHz reference clock for synthesizer output |
| $V_{SS1}$ | 15 | – | – | supply | negative supply voltage 1 |
| $V_{DD\_RF}$ | 16 | – | – | supply | positive supply voltage for RF interface level shifters |
| $V_{DD3V\_1}$ | 17 | – | – | supply | positive supply voltage 1 (+3 V) |
| SLICE_CTR | 18 | O | L | ISP2DRF3 | switch slicer time constant output |
| R_PWR | 19 | O | H | ISP2DRF3 | switch receiver power output |
| R_DATAP | 20 | I | – | ANAIOD2 | positive input for receiver data |
| R_DATAM | 21 | I | – | ANAIOD2 | negative input for receiver data |
| R_ENABLE | 22 | O | H | ISP2DRF3 | enable receiver output |
| RSSI_AN | 23 | I | – | ANAIOD1 | analog input for RSSI measurement |
| VANLI | 24 | I | – | ANAIOD1 | analog input to ADC |
| VBAT | 25 | I | – | ANAIOD1 | analog input for battery voltage measurement |
| CLK3 | 26 | O | L | ISP2DPES | 3.456 MHz clock output for external ADPCM codec |
| DCK | 27 | I/O | input | ISF2DPES<br>ISF2UPES | ADPCM output or IOM®-2 data clock input/output<br>(ISF2UPES in PCD5090/xxx, PCA5097/xxx) |
| DI | 28 | I | – | DIPP0PES | ADPCM or IOM®-2 data input |
| FS1 | 29 | I/O | input | ISF2DPES<br>ISF2UPES | 8 kHz framing input/output<br>(ISF2UPES in PCD5090/xxx, PCA5097/xxx) |
| DO | 30 | O | off | ISI8DPES | ADPCM or IOM®-2 data output |
| XTAL2 | 31 | O | running | ANAIOD1 | crystal oscillator output |
| XTAL1 | 32 | I | – | ANAIOD1 | crystal oscillator input |
| VANLO | 33 | O | 1.0 V | ANAIOD1 | analog output from DAC |
| $V_{SSO}$ | 34 | – | – | supply | negative supply voltage for the oscillator |
| $V_{DDO}$ | 35 | – | – | supply | positive supply voltage for the oscillator |

| SYMBOL | PIN | I/O | STATE AFTER RESET | PIN TYPE | PIN DESCRIPTION |
|---|---|---|---|---|---|
| LIFM | 36 | I | 0.7 V | ANAIOD1 | negative input from line interface |
| LIFP | 37 | I | 0.7 V | ANAIOD1 | positive input from line interface |
| $V_{SSA}$ | 38 | – | – | supply | negative supply voltage for analog circuits |
| MICM | 39 | I | 0.7 V | ANAIOR1 | negative input from microphone |
| MICP | 40 | I | 0.7 V | ANAIOR1 | positive input from microphone |
| VMIC | 41 | O | off | ANAIOD1 | positive microphone supply voltage (+2 V) |
| $V_{ref}$ | 42 | O | 2.0 V | ANAIOD1 | reference voltage (+2 V) |
| VBGP | 43 | O | 1.25 V | ANAIOR1 | bandgap output voltage (+1.25 V) |
| $V_{DDA}$ | 44 | – | – | supply | positive supply voltage for analog circuits |
| EARM | 45 | O | 1.4 V | ANAIOD1 | negative output to earpiece |
| EARP | 46 | O | 1.4 V | ANAIOD1 | positive output to earpiece |
| EN_WATCHDOG | 47 | I | – | DIUP0PES | Watchdog Timer enable input |
| P1.0 | 48 | I/O | H | ISQ2CPES | bidirectional 80C51 port pin |
| P1.1 | 49 | I/O | H | ISQ2CPES | bidirectional 80C51 port pin |
| P1.2 | 50 | I/O | H | ISQ2CPES | bidirectional 80C51 port pin |
| GP_CLK7 | 51 | O | L | ISP2DPES | general purpose 6.912 MHz output |
| DPLL_DATA | 52 | O | L | ISP2DPES | data after clock recovery network |
| R_SLICED | 53 | O | L | ISP2DPES | R_DATA comparator output |
| $V_{DD5V\_1}$ | 54 | – | – | supply | positive supply voltage 1 for the +5 V interface |
| P1.3 | 55 | I/O | H | ISQ2CPES | bidirectional 80C51 port pin |
| P1.4 | 56 | I/O | H | ISQ2CPES | bidirectional 80C51 port pin |
| P1.5 | 57 | I/O | H | ISQ2CPES | bidirectional 80C51 port pin |
| P1.6 | 58 | I/O | off | ISI8DPES | bidirectional 80C51 port pin |
| P1.7 | 59 | I/O | off | ISI8DPES | bidirectional 80C51 port pin |
| $V_{DD3V\_2}$ | 60 | – | – | supply | positive supply voltage 2 (+3 V) |
| BZM | 61 | O | L | ANAIOD2 | negative buzzer output |
| BZP | 62 | O | L | ANAIOD2 | positive buzzer output |
| $V_{SS2}$ | 63 | – | – | supply | negative supply voltage 2 |
| $V_{SS3}$ | 64 | – | – | supply | negative supply voltage 3 |
| P3.0 | 65 | I/O | H | ISQ2CPES | bidirectional 80C51 port pin |
| P3.1 | 66 | I/O | H | ISQ2CPES | bidirectional 80C51 port pin |
| P3.2 | 67 | I/O | H | ISQ2CPES | bidirectional 80C51 port pin |
| P3.3 | 68 | I/O | H | ISQ2CPES | bidirectional 80C51 port pin |
| P3.4 | 69 | I/O | H | ISQ2CPES | bidirectional 80C51 port pin |
| P3.5 | 70 | I/O | H | ISQ2CPES | bidirectional 80C51 port pin |
| P3.6 | 71 | I/O | H | ISQ2CPES | bidirectional 80C51 port pin |
| P3.7 | 72 | I/O | H | ISQ2CPES | bidirectional 80C51 port pin |
| P2.0 | 73 | I/O | H | ISQ2CPES | bidirectional 80C51 port pin |
| P2.1 | 74 | I/O | H | ISQ2CPES | bidirectional 80C51 port pin |

| SYMBOL | PIN | I/O | STATE AFTER RESET | PIN TYPE | PIN DESCRIPTION |
|---|---|---|---|---|---|
| P2.2 | 75 | I/O | H | ISQ2CPES | bidirectional 80C51 port pin |
| A16 | 76 | O | L | ISP4DPES | address bit 16 for 128 kbytes external program memory |
| $V_{DD5V\_2}$ | 77 | – | – | supply | positive supply voltage 2 for the +5 V interface |
| $V_{SS4}$ | 78 | – | – | supply | negative supply voltage 4 |
| TST1 | 79 | I | – | DIDP0PES | test input 1 |
| TST2 | 80 | I | – | DIDP0PES | test input 2 |
| P2.3 | 81 | I/O | H | ISQ2CPES | bidirectional 80C51 port pin |
| P2.4 | 82 | I/O | H | ISQ2CPES | bidirectional 80C51 port pin |
| P2.5 | 83 | I/O | H | ISQ2CPES | bidirectional 80C51 port pin |
| P2.6 | 84 | I/O | H | ISQ2CPES | bidirectional 80C51 port pin |
| P2.7 | 85 | I/O | H | ISQ2CPES | bidirectional 80C51 port pin |
| $\overline{PSE}$ | 86 | O | H | ISQ2CPES | program store enable (80C51); active LOW |
| ALE | 87 | O | H | ISQ4CPES | address latch enable (80C51) |
| $\overline{EA}$ | 88 | I | – | ISF2DPES | external access enable (80C51); active LOW |
| $V_{SS5}$ | 89 | – | – | supply | negative supply voltage 5 |
| $V_{DD5V\_3}$ | 90 | – | – | supply | positive supply voltage 3 for the +5 V interface |
| P0.7 | 91 | I/O | off<br>H | ISP2DPES<br>ISQ2CPES | bidirectional 80C51 port pin<br>(ISQ2CPES in PCD5090/xxx, PCA5097/xxx) |
| P0.6 | 92 | I/O | off<br>H | ISP2DPES<br>ISQ2CPES | bidirectional 80C51 port pin<br>(ISQ2CPES in PCD5090/xxx, PCA5097/xxx) |
| P0.5 | 93 | I/O | off<br>H | ISP2DPES<br>ISQ2CPES | bidirectional 80C51 port pin<br>(ISQ2CPES in PCD5090/xxx, PCA5097/xxx) |
| P0.4 | 94 | I/O | off<br>H | ISP2DPES<br>ISQ2CPES | bidirectional 80C51 port pin<br>(ISQ2CPES in PCD5090/xxx, PCA5097/xxx) |
| P0.3 | 95 | I/O | off<br>H | ISP2DPES<br>ISQ2CPES | bidirectional 80C51 port pin<br>(ISQ2CPES in PCD5090/xxx, PCA5097/xxx) |
| P0.2 | 96 | I/O | off<br>H | ISP2DPES<br>ISQ2CPES | bidirectional 80C51 port pin<br>(ISQ2CPES in PCD5090/xxx, PCA5097/xxx) |
| P0.1 | 97 | I/O | off<br>H | ISP2DPES<br>ISQ2CPES | bidirectional 80C51 port pin<br>(ISQ2CPES in PCD5090/xxx, PCA5097/xxx) |
| P0.0 | 98 | I/O | off<br>H | ISP2DPES<br>ISQ2CPES | bidirectional 80C51 port pin<br>(ISQ2CPES in PCD5090/xxx, PCA5097/xxx) |
| M_RESET | 99 | I | – | DIDP0PES | master reset input (Schmitt trigger) |
| RESET_OUT | 100 | O | H | ISF2DPES | reset output |

## 6 FUNCTIONAL DESCRIPTION

The PCD509x is a family of single-chip controllers, designed for use in Digital Enhanced Cordless Telecommunications systems (DECT). The family is designed for minimum component-count and minimum power consumption. All controllers include an embedded 80C51 microcontroller with on-chip memory and $I^2C$-bus interface. The Philips DECT RF interface is implemented. The Burst Mode Logic (BML) performs the time-critical MAC layer functions for applications in DECT handsets and base stations. The ADPCM transcoding is in compliance with the CCITT recommendation G.721 and includes receive and transmit filters.

The PCD5095 is designed for business systems, PABX and WLL. Two modes can be selected: bidirectional conversion of three ADPCM channels based on linear PCM format, the second mode copies four ADPCM samples, without data processing, into two IOM®-2 data buffers and vice versa. In both modes the DSP controls the bidirectional data flow from the radio interface and the IOM®-2 interface. The 80C51 controls the DECT protocol and the IOM®-2 interface.

The data flow between radio, DSP and IOM®-2 is described in the *"PCD5095 DSP user manual"*. Basically the System Data RAM (SDR), the shared memory with inbound and outbound speech buffers, is the interface to the DSP and to the radio. Depending on the selected mode the DSP processes the data stored in the SDR. The speech buffers are 40 bytes long and each buffer can hold 80 ADPCM-coded speech samples.

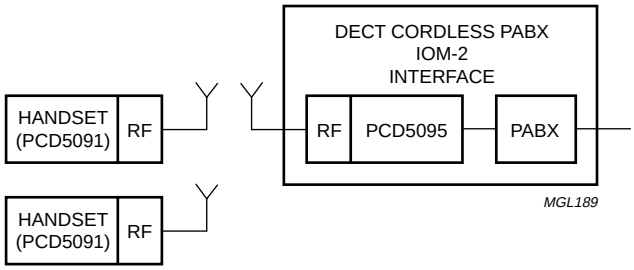
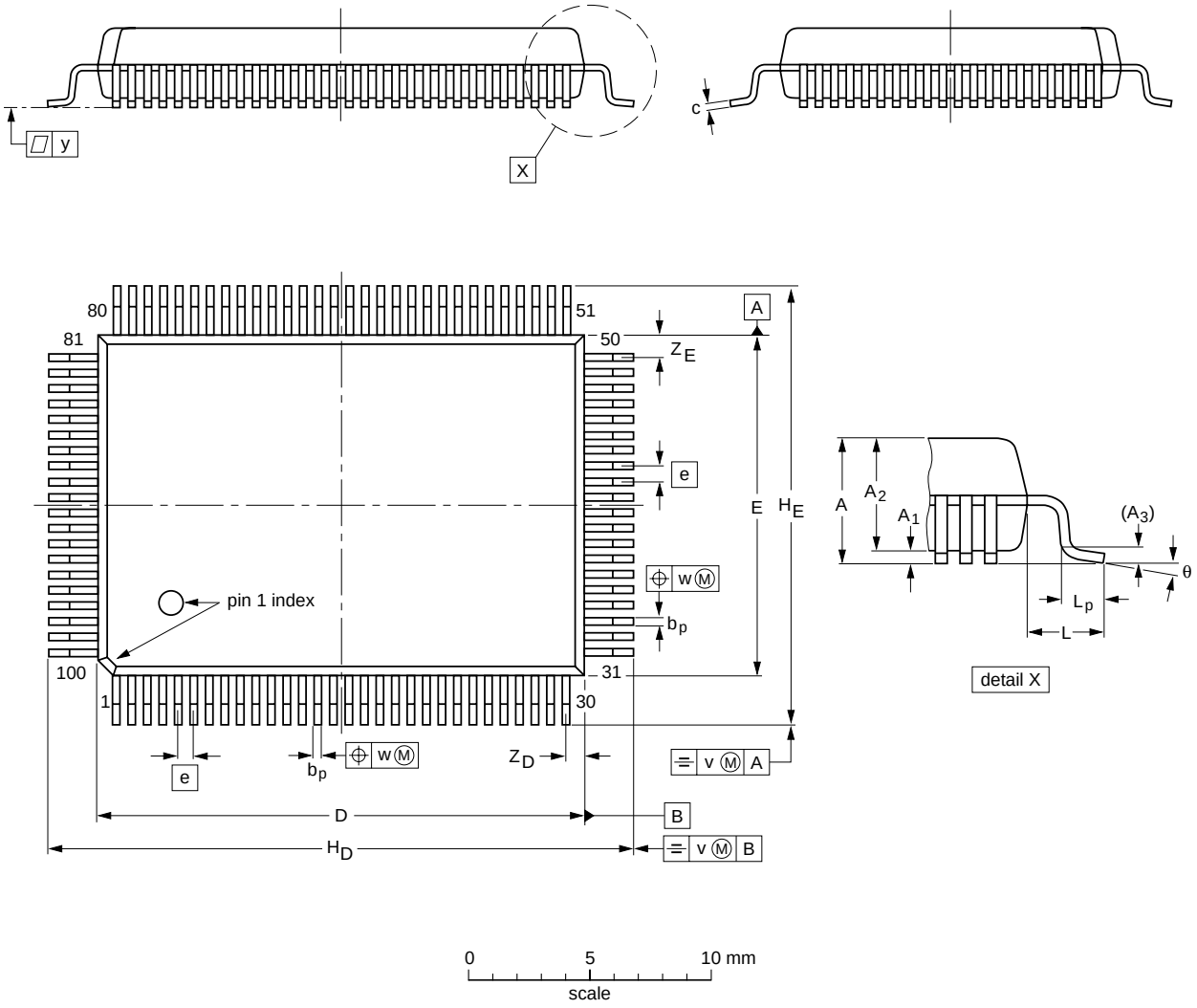



Fig.3 PCD5095 for PABX.

## 7 PACKAGE OUTLINE

**QFP100: plastic quad flat package; 100 leads (lead length 1.95 mm); body 14 x 20 x 2.8 mm** **SOT317-2**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(1)}$ | e | $H_D$ | $H_E$ | L | $L_p$ | v | w | y | $Z_D^{(1)}$ | $Z_E^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 3.20 | 0.25<br>0.05 | 2.90<br>2.65 | 0.25 | 0.40<br>0.25 | 0.25<br>0.14 | 20.1<br>19.9 | 14.1<br>13.9 | 0.65 | 24.2<br>23.6 | 18.2<br>17.6 | 1.95 | 1.0<br>0.6 | 0.2 | 0.15 | 0.1 | 0.8<br>0.4 | 1.0<br>0.6 | $7^o$<br>$0^o$ |

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT317-2 | | | | | | ~~95-02-04~~<br>97-08-01 |

## 8 SOLDERING

### 8.1 Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

### 8.2 Reflow soldering

Reflow soldering techniques are suitable for all QFP packages.

The choice of heating method may be influenced by larger plastic QFP packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information, refer to the Drypack chapter in our *"Quality Reference Handbook"* (order code 9397 750 00192).

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 50 and 300 seconds depending on heating method. Typical reflow peak temperatures range from 215 to 250 °C.

### 8.3 Wave soldering

Wave soldering is **not** recommended for QFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

| **CAUTION** |
| --- |
| **Wave soldering is NOT applicable for all QFP packages with a pitch (e) equal or less than 0.5 mm.** |

**If wave soldering cannot be avoided, for QFP packages with a pitch (e) larger than 0.5 mm, the following conditions must be observed:**

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

### 8.4 Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

## 9 DEFINITIONS

| **Data sheet status** | |
|---|---|
| Objective specification | This data sheet contains target or goal specifications for product development. |
| Preliminary specification | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification | This data sheet contains final product specifications. |
| Short-form specification | The data in this specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook. |
| **Limiting values** | |
| Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability. | |
| **Application information** | |
| Where application information is given, it is advisory and does not form part of the specification. | |

## 10 LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

## 11 PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

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